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April 17, 2004

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APPLICATION NUMBER: *60/449,049*
FILING DATE: *February 21, 2003*
RELATED PCT APPLICATION NUMBER: *PCT/US04/04676*

By Authority of the
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(Signature of Person Mailing Paper or Fee)

Michael K. Kinney

(Typed or Printed Name of Person Mailing Paper or Fee)

PROVISIONAL APPLICATION FOR PATENT COVER SHEET

This is a request for filing a PROVISIONAL APPLICATION FOR PATENT under 37 CFR 1.53(c).

Docket No. 102402-100			Type a plus (+) Inside this box 6	+
INVENTOR(s)/APPLICANT(s)				
LAST NAME	FIRST NAME	MIDDLE INITIAL	RESIDENCE (CITY AND EITHER STATE OR FOREIGN COUNTRY)	
JUSKEY	Frank	J.	Dublin, CA	
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TITLE OF INVENTION (280 characters max)

LEAD FRAME WITH INCLUDED PASSIVE DEVICES

CORRESPONDENCE ADDRESS

Customer Number:

27267

PATENT TRADEMARK OFFICE

Enclosed Application Parts (check all that apply)

[X] Specification (claims & abstract)	Number of pages [25]	
[X] Drawing(s)	Number of Sheets [1]	[X] Other (specify) _Return post card_

METHOD OF PAYMENT OF FILING FEES FOR THIS PROVISIONAL APPLICATION FOR PATENT (check one)

[ ] A check or money order is enclosed to cover the filing fees Filing Fee Amount(s) $160.00

[X] The Commissioner is hereby authorized to charge filing fees and credit Deposit Account No. 23-1665

The invention was made by an agency of the United States Government or under a contract with an agency of the United States Government.

[X] No [ ] Yes, the name of the U.S. Government agency and the Government contract number is

Respectfully submitted,

SIGNATURE: Date: February 21, 2003

TYPED or PRINTED NAME: Michael K. Kinney Registration No. 42,740

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LEAD FRAME WITH INCLUDED PASSIVE DEVICES

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates generally to semiconductor manufacture and, more particularly, to lead frame packaging having semiconductor dies and passive devices co-located on the lead frame.

2. Description of the Related Art

In a conventional semiconductor die package a housing encases the semiconductor die to prevent damage to the die from exposure to the environment. The housing may be hermetically sealed, encased in plastic, or otherwise protected from the environment. In many electronic assemblies, passive components such as, for example, capacitors, inductors and resistors, are interconnected with semiconductor die packages to provide desired functions. Heretofore, most of these passive components could not be integrated within an encased die package in a cost effective manner.

It is desirable from both a manufacturer's and user's standpoint that electronic assemblies require as few as possible external connections since such connections increase manufacturing costs (that are ultimately passed to the user) and can introduce noise to the package as signals are propagated from external components.

Accordingly, the inventors have realized that a need exists for an improved semiconductor die package including a cost effective method for placing passive components close to a semiconductor die and for encasing the passive components and die in a single package.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a perspective, partial cross sectional view of a multi-component electronic assembly configured and operating in accordance with one embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. 1 shows an electronic package 10 including a semiconductor die 20 having one or more integrated circuit elements and a lead frame 30 supporting the die 20. Commonly, the die 20 is of nominally rectangular or, more particularly square plan that is coupled to a printed circuit

board (not shown). The lead frame 30 is comprised of a stamped or etched metallic structure and includes a plurality of conductive leads 32.

As shown in FIG. 1, the semiconductor die 20 is attached to the lead frame 30 by, for example, a conductive adhesive 40 (e.g., metal filled epoxy) disposed between the lead frame 30 and a lower surface of the die 20. It should be appreciated that the die 20 may also be attached to the lead frame 30 by solder.

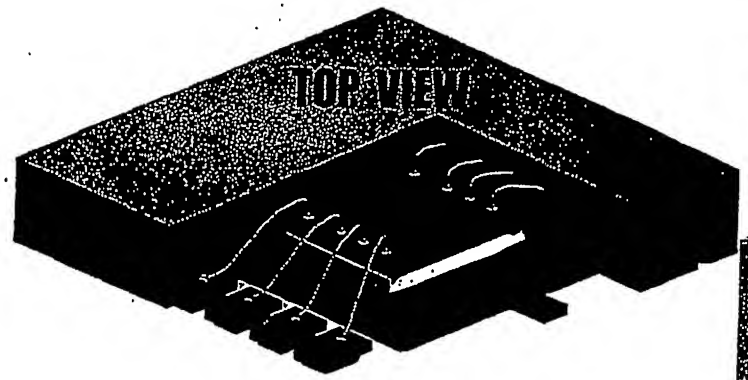
The package 10 includes a plurality of bond pads 50, at least some of which provide electrical communication between the semiconductor die 20 and an apparatus in which the electronic package 10 is installed (e.g., via connection to the printed circuit board). For example, the die 20 may be electrically connected to the bond pads 50 by appropriate means such as wire bonding. FIG. 1 illustrates a plurality of wires 60 coupling the die 20 to the bond pads 50.

In accordance with the present invention, passive devices 80 such as, for example, capacitors, inductors and resistors, are attached to the lead frame 30 by, for example, solder 90. In the one embodiment, the semiconductor die 20, pads 50, wires 60, passive devices 80 and inboard portions of the lead frame 30 are encapsulated within an encapsulant 70 molded in situ to provide physical and environmental protection of the components within the assembly 10. Preferably, undersides of the bond pads 50 are exposed through the encapsulant to permit electrical contact with the apparatus in which the package is installed (e.g., via connection to the printed circuit board). It should be appreciated that an equivalent assembly may be sealed in a metal or ceramic encasing.

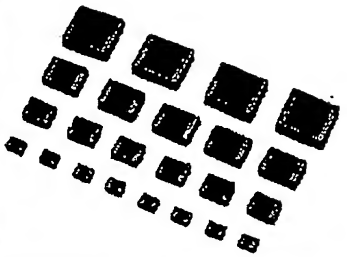
As illustrated in FIG. 1, the passive devices 80 are located in close proximity to the die 20 yielding a component assembly having an overall size that is less than conventional multi-component die packages. The inventors have realized that the inventive configuration demonstrates faster electrical connective between components as there are fewer external leads and shorter wire lengths between the components. Preferably, the assembly 10 is a drop-in replacement to dual flat non-leaded assemblies such as, for example, small outline integrated circuits (SOIC), thin shrink small outline packages (TSSOP), quarter size outline packages (QSOP), and the like.

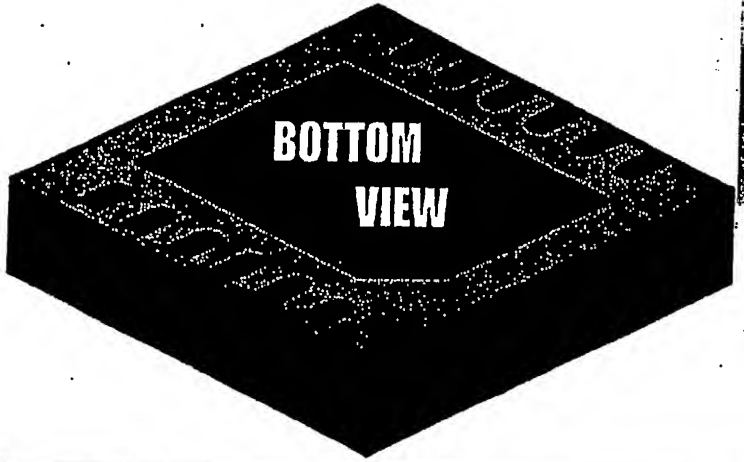
Some features and functions of an exemplary embodiment of the present invention are described below.

DUAL FLAT NON-LEADED



DFN



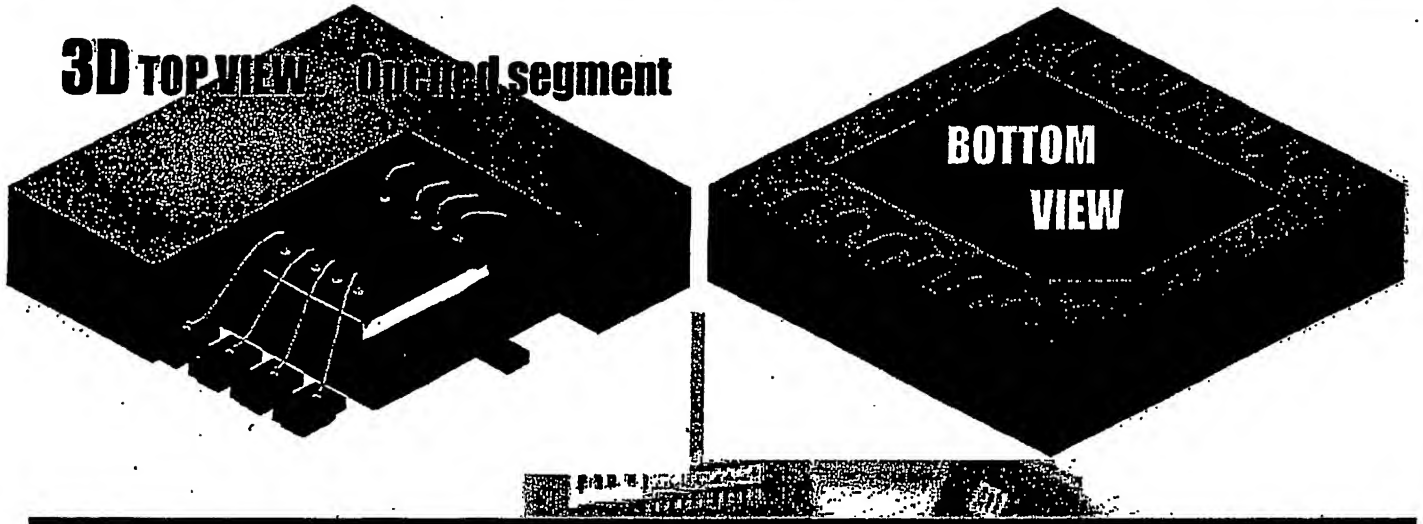


Dual-sided QFN

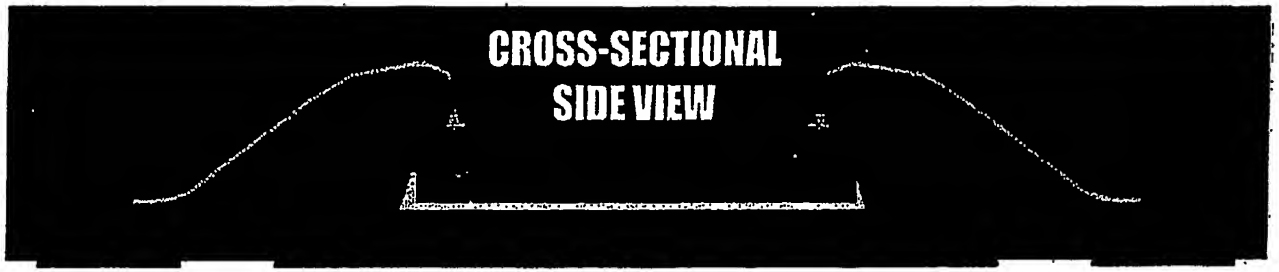
With / without
PRESSES

A MIGRATION PATH FOR SOIC, TSSOP, QSOP.....

DFN : A DUAL-SIDED QFN



THERMALLY SUPERIOR	:	WITH DIE-PAD EXPOSED TO PCB MOUNTING
ELECTRICALLY FASTER	:	NO EXTERNAL LEADS & SHORTER WIRE LENGTH



DFN / DFN+ OFFERS

SOIC / TSSOP

THIN	LOW INDUCTIVE PARASITIC LIKE QFN
LEADLESS	ELIMINATES BOARD COPLANARITY ISSUES
PIN-TO-PIN	DIRECT POSITIVE REPLACEMENT
Same Board-Attach	EASIER SMT EQUIPMENT LEAD ALIGNMENT
Better Materials	IMPROVED AND CONSISTENT MATERIAL SET
LEAD-FREE PACKAGE	READY TO ADOPT LEAD FREE PACKAGE

MULTI-DIE AND PASSIVE COMPATABLE PACKAGING ALTERNATIVE

DFN / DFN+ PACKAGE OFFERINGS

BODY SIZE (mm x mm)	LEAD COUNT	DIE PAD (mm x mm)	MAXIMUM DIE SIZE Without Ground (mm x mm)	MAXIMUM DIE SIZE With Ground Bond (mm x mm)
2 x 4	4	0.80	0.55	Not Feasible
3 x 5	4, 6, 8	1.50	1.25	0.74
4 x 6	6, 8, 10, 12	2.50	2.25	1.74
5 x 7	10, 12, 14, 16	3.50	3.25	2.74
6 x 8	10, 14, 18, 20	4.50	4.25	3.74
7 x 9	14, 16, 22, 24	5.00	4.75	4.24
8 x 10	16, 18, 20, 22, 24, 26, 28	6.50	6.25	5.74
9 x 11	22, 24, 28, 30, 32	7.75	7.50	7.00
10 x 12	32, 34, 38, 40	8.25	8.00	7.50

- FLIP CHIP OFFERED USING COPPER PILLAR BUMPS WITH SOLDER CAP (APS LICENSE)
- TOOLING LEAD-TIME FOR NEW BODY SIZE : Leadframe = 4 Wks & Saw Jigs = 6 Wks

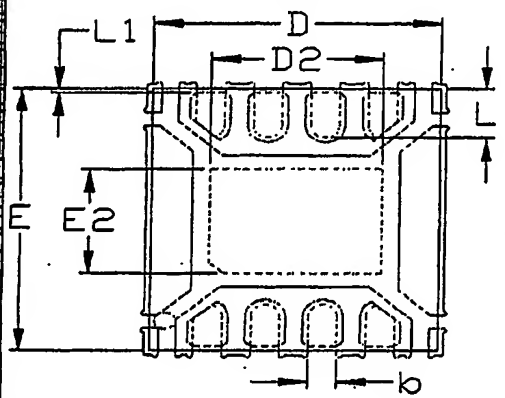
DFN JEDEC : WIRE-BOND

JEDEC STANDARD PACKAGES		
PACKAGE SIZE	SQUARE PACKAGES PITCH	LEAD COUNTS
1.5X1.5		4
2.0X2.0		6
2.0X2.0	0.65	8
2.5X2.5		8,10
2.5X2.5	0.80	6,8,10
3.0X3.0		8,10
3.0X3.0	0.65	8,10
3.0X3.0	0.80	6,8,10
3.5X3.5		10,12
4.0X4.0		10,12,14
4.0X4.0	0.80	6,8,10
5.0X6.0		16,18
5.0X5.0	0.80	8,10

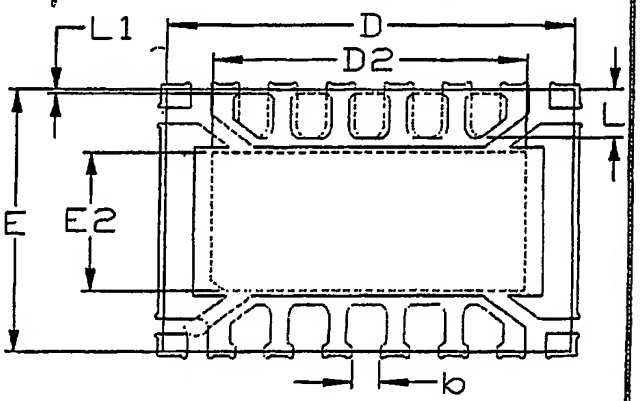
PACKAGE SIZE	DFN2 PACKAGES PITCH	LEAD COUNTS
2.0X2.5		6
2.0X2.5	0.65	4
2.5X3.0		8
2.5X3.0	0.80	6
3.0X4.0		10
3.0X4.0	0.80	8
4.0X5.0		14
4.0X5.0	0.80	10

PACKAGE SIZE	DFN3 PACKAGES PITCH	LEAD COUNTS
1.5X1.0		4
2.0X1.0		4,6
2.0X1.5		4,6
2.5X1.5		6,8
2.5X2.0		4,6,8
3.0X1.5		8,10
3.0X2.0		9,10
3.0X2.0	0.65	8
3.0X2.5		8,10
3.5X2.5		10,12
3.5X3.0		10,12
4.0X3.0		10,12,14
5.0X3.0		16,18
5.0X4.0		14,16,18

TYPE 1



TYPE 2

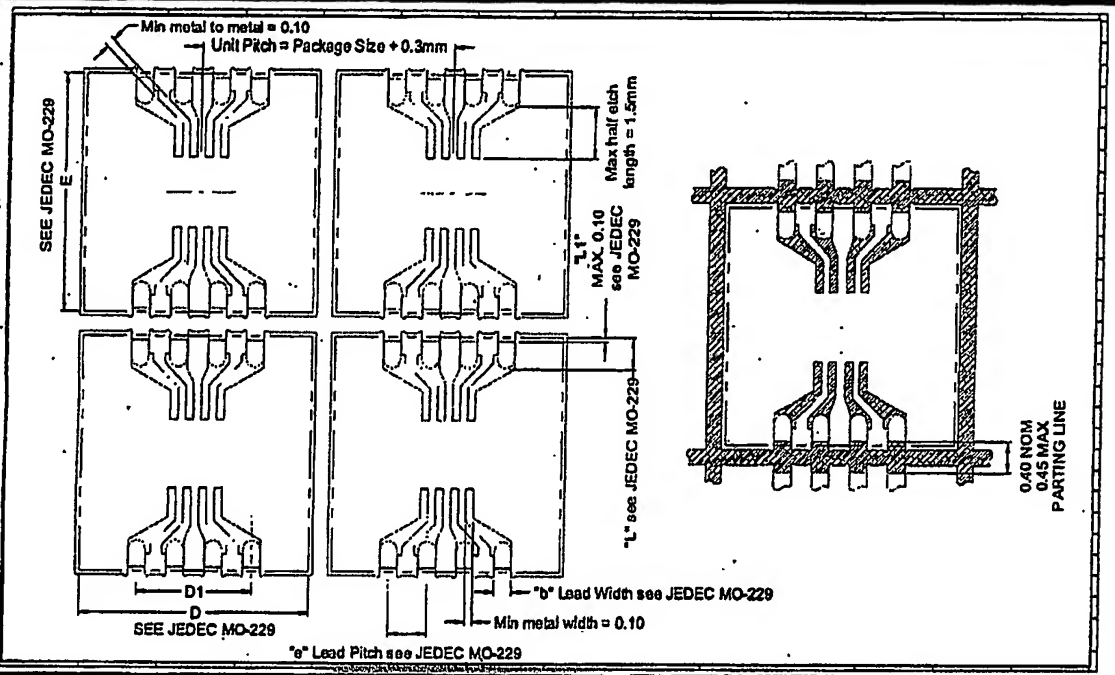


JEDEC Variation: VDED

SYMBOL	MILLIMETER Min	Nom	Max	INCH Min	Nom	Max
A	0.80	0.80	1.00	.031	.035	.039
A2	0.00	0.65	1.00	.000	.026	.039
b	0.18	0.25	0.30	.007	.010	.012
D		2.50 BSC			.098 BSC	
(ND-1)e		1.50 BSC			.059 BSC	
D2	0.00	1.50	1.60	.000	.059	.063
E		3.00 BSC			.118 BSC	
E2	1.10	1.20	1.30	.043	.047	.051
e		0.50 BSC			.020 BSC	
L	0.45	0.55	0.65	.018	.022	.026
N		8				
ND		4				
MAX DIE PAD		2.25 X 1.50			0.089 X 0.059	
MAX DIE		1.50 X 1.25			0.059 X 0.049	
NON JEDEC MAX DIE WITH DOWN BONDS		1.00 X 0.95			0.039 X 0.037	
PITCH		0.50				

WIRE-BOND DESIGN RULES	25um Wire	33um Wire
Max. wire length	3.00mm	3.80mm
Max wire length over silicon	0.38mm	0.89mm
Max wire loop height	0.20mm	0.25mm
Min wire loop height	0.10mm	0.125mm
Min die to diepad edge distance without wire bonds	0.125mm	0.125mm
Min die to diepad edge distance with wire bonds	0.38mm	0.50mm
Max die to diepad edge distance with wire bonds	1.27mm	1.65mm
Min die to die distance without down bonds	0.50mm	0.50mm
Min die to die distance with down bonds	0.75mm	0.75mm
Min bond pad opening	83.5um	70um
Min inline bond pad pitch	70um	70um
Max 4 bond wires per lead in production run		
Lead Area/.0288 = Number of wires per lead in production run		
Lead Area/.0153 = Number of wires per lead in engineering run		
Bond wire angle = or > 45 degrees		
Distance between wires = or > wire diameter		
Cantilever Min should be .05mm		
Cantilever can be Max possible when no down bonds		
Cantilever Max is .15mm when down bonds		
Cantilever Nom. on die pad is .15mm and .05mm on lead		
Recommended wafer thickness is 8 - 10 mils		

DFN JEDEC : FLIP-CHIP

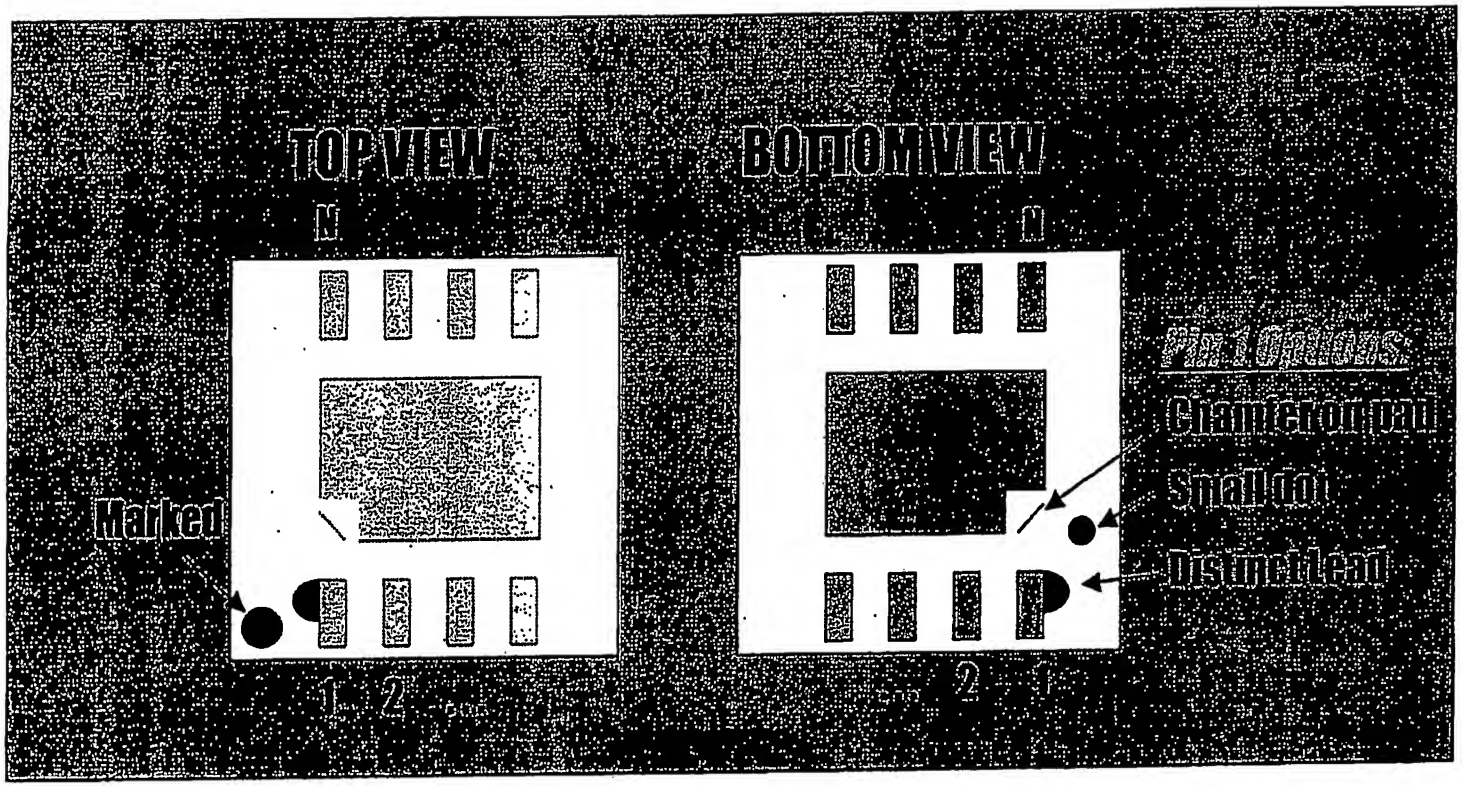


FLIP-CHIP DESIGN RULES	
Max. half etch cantilever length	1.50 mm
Min. metal to metal distance	0.10 mm
Min. metal width	0.10 mm
Recommended wafer thickness	8 - 10 mils

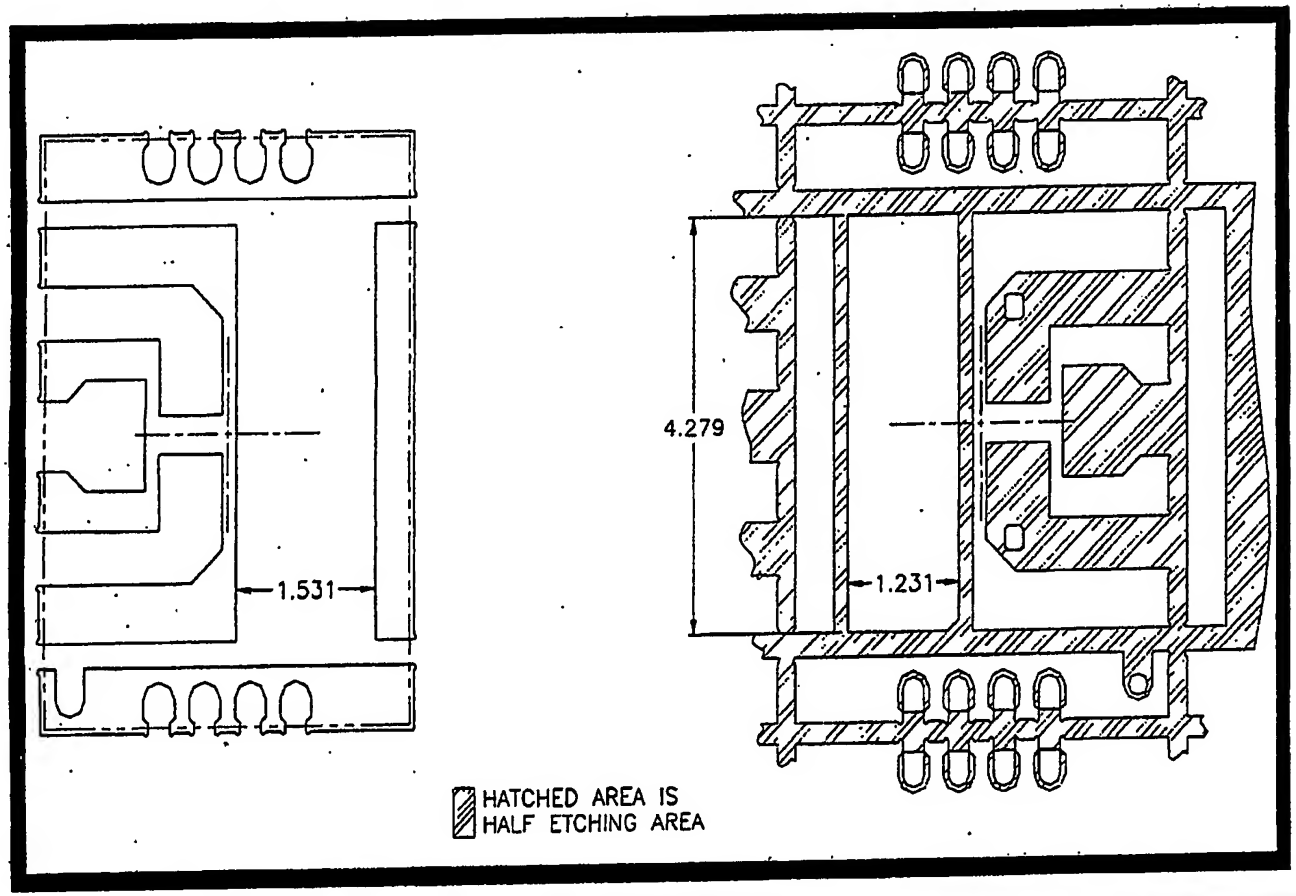
AIT STANDARD FLIP-CHIP MATERIALS	
Leadframe:	
	Copper 194 FH or C7025
	Half-Etching
	Back side tape
	Pre-Plated (NiPdAu) or Silver spot
Mold Compound:	
	EME 7730LC
	G770
	CEL 9920
Saw Blade:	
	Mitsubishi D325M or equivalent

DFN / DFN+ PIN-OUT

PIN "1" IDENTIDICATION : (JEDEC MO-229)



DFN+ LEADFRAME CONFIGURATION



384 UNITS PER STRIP { 70mm x 250mm } IN FOUR 12 x 8 PANELS

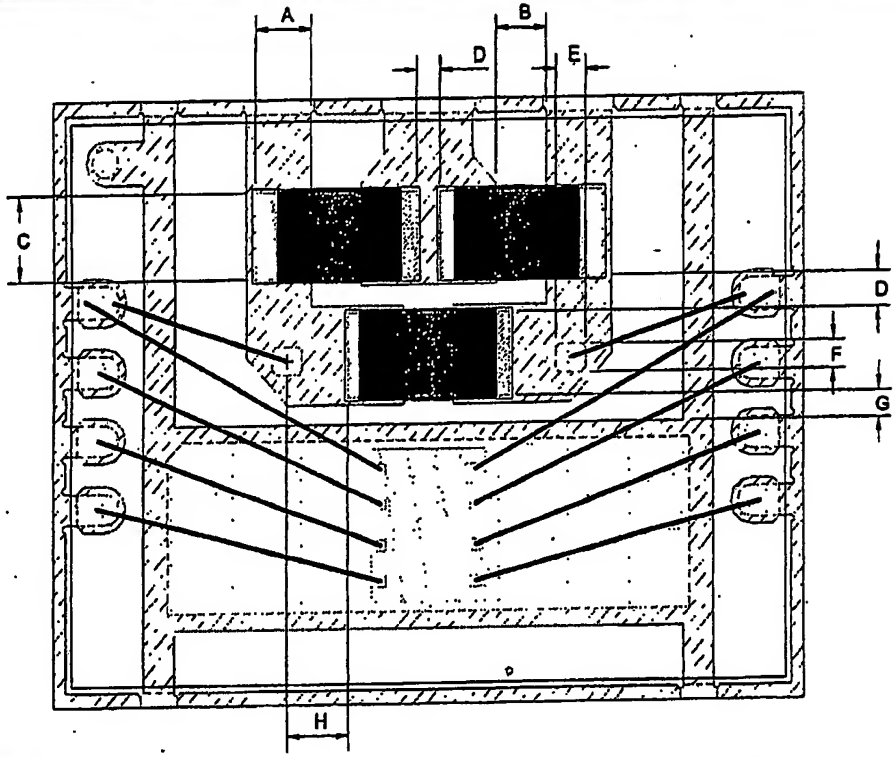
DFN+ Passives



Global Part Number	GRP155B11H102KA01B
Previous Part Number	GRM36B102K50
Length L	1.00mm ±0.05mm
Width W	0.50mm ±0.05mm
Thickness T	0.50mm ±0.05mm
Electrode e	0.15 to 0.30mm
Electrode Gap g	0.40mm min.
TC Code (Standard)	B (JIS)
Capacitance Change	±10%
TC Change Correction	
Temperature Range	-25 to 85°C
Capacitance	1000pF ±10%
Rated Voltage	50Vdc
Soldering Method	Reflow
Recommended Parts	Recommended
EIA	0402

Global Part Number	LQG18HN10NJ00B
Previous Part Number	LQG11A10NJ00
Inductance	10nH
Tolerance of Inductance	±5%
Test Frequency	100MHz
Rated Current	300mA
Max. of DC resistance	0.30ohm
Typ. of DC resistance	
Q (min.)	12
Test Frequency	100MHz
Self Resonance Frequency	3500MHz min.
Min. of Operating Temp.	-40°C
Max. of Operating Temp.	+85°C
Length	1.6mm
Width	0.8mm
Thickness	0.8mm
EIA	0603
Weight	0.003g (Typ.)

DFN+ WITH PASSIVES

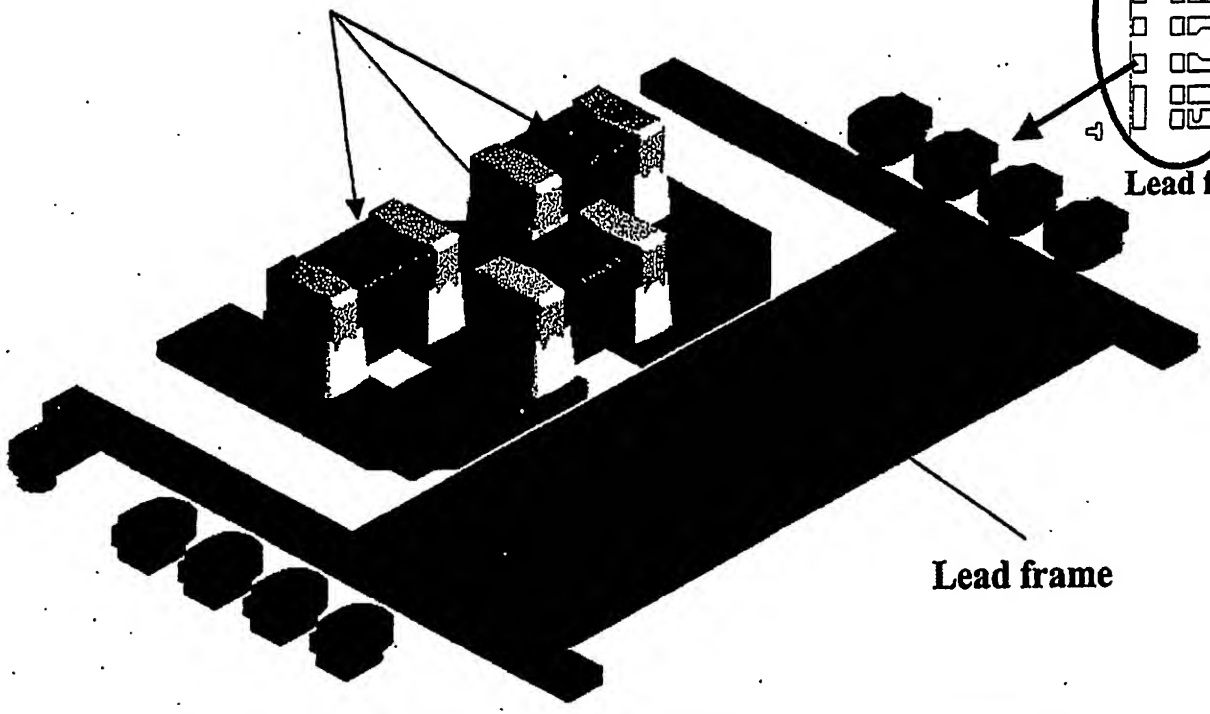


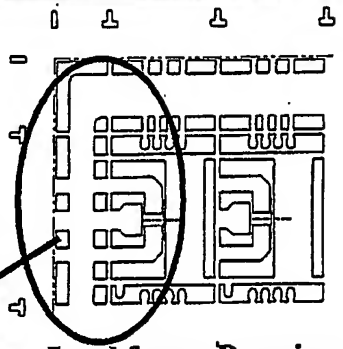
Component Size (All Dimensions are in microns)	A Component Pad Length	B Component Pad Space	C Component Pad Width	D Component Pad to Component Pad Minimum	E Support Pad Length	F Support Pad Width	G Component Pad to Die Flag	H Wire Bond to Pad
Chip Component 0402	470	420	600	200	300	250	200	400
Chip Component 0201	270	260	350	200	300	250	200	400

DFN+ PASSIVE ATTACH

PASSIVES TO BE MOUNTED AT LOCAL SUB-CONTRACTOR

PASSIVES (0201 / 0402 / 0603)





Lead frame Drawing extract

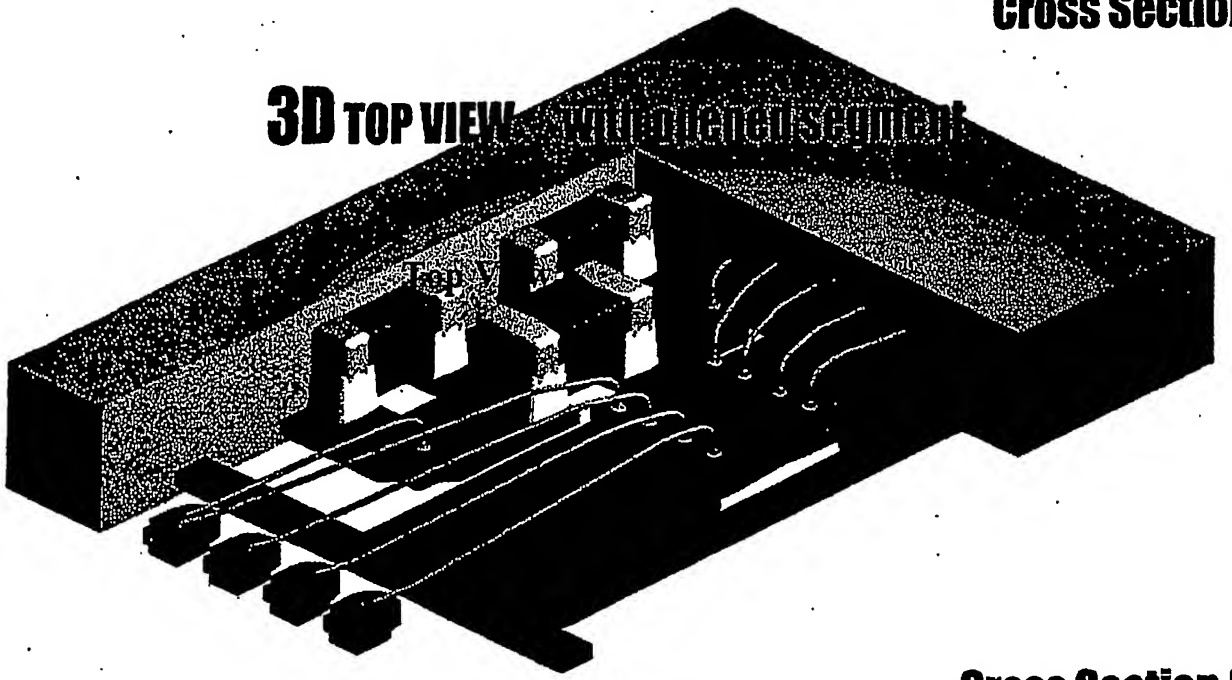
Lead frame

PASSIVES MOUNTED FRAMES TO BEGIN CHIP ASSEMBLY / TEST

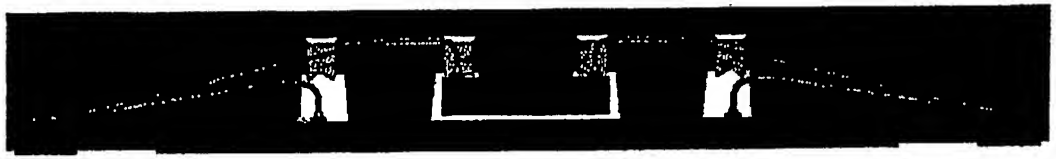
DFN+ CONSTRUCTION

Cross Section (sort side)

3D TOP VIEW with dielectric segment



Cross Section (long side)



DFN+ Challenges

- Wafer Handling
- Multiple Dies
- MOS Capacitors
- Gallium-Arsenide
- Multiple Passives
- Wafer Handling

DFN Material Set

COMPONENT	DIMENSION
MOLD THICKNESS	0.90/0.75 mm
DIE THICKNESS	0.20-0.25 mm
LEADFRAME	0.20 mm
WIRE LOOP	0.15 mm

MARKING / SHIPPING

- Laser Marking
- Tray Tubes or Tape & Reel

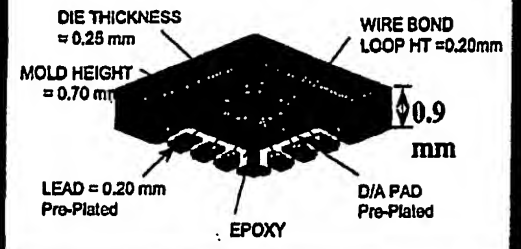
BILL OF MATERIALS

Die Attach	CRM 1064
Mold Compound	CEL 9220, *T*130, *T*10
Gold Wire	25 um
Etched Leadframe	CU194FH
Leadframe Finish	o Sn:Pb (85:15) o Sn (100%) o Preplated (Ni-Pd-Au) (1.3u, .05-.2u, .002-.02u)

AIT IS DFN READY !

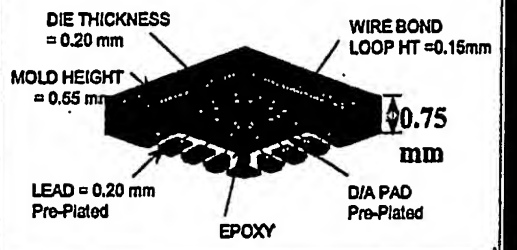
AIT QFN

VFQFP-N, MO-220
0.9 mm PACKAGE HEIGHT



AUTOLINE

WFQFP-N, MO-220
0.75 MM PACKAGE HEIGHT

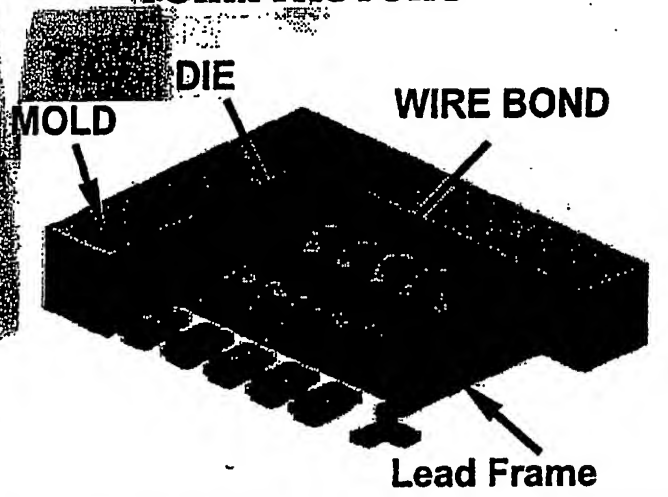


QUALIFIED

READY

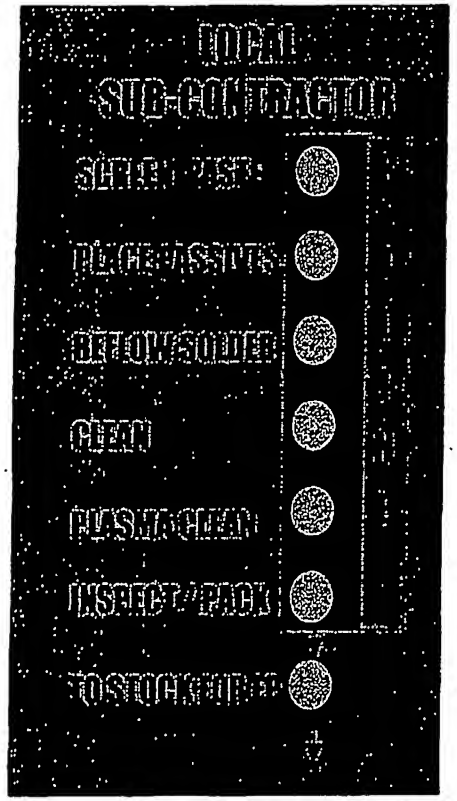
DFN

FINER FEATURES FOR DUAL-SIDED FORM FACTORS



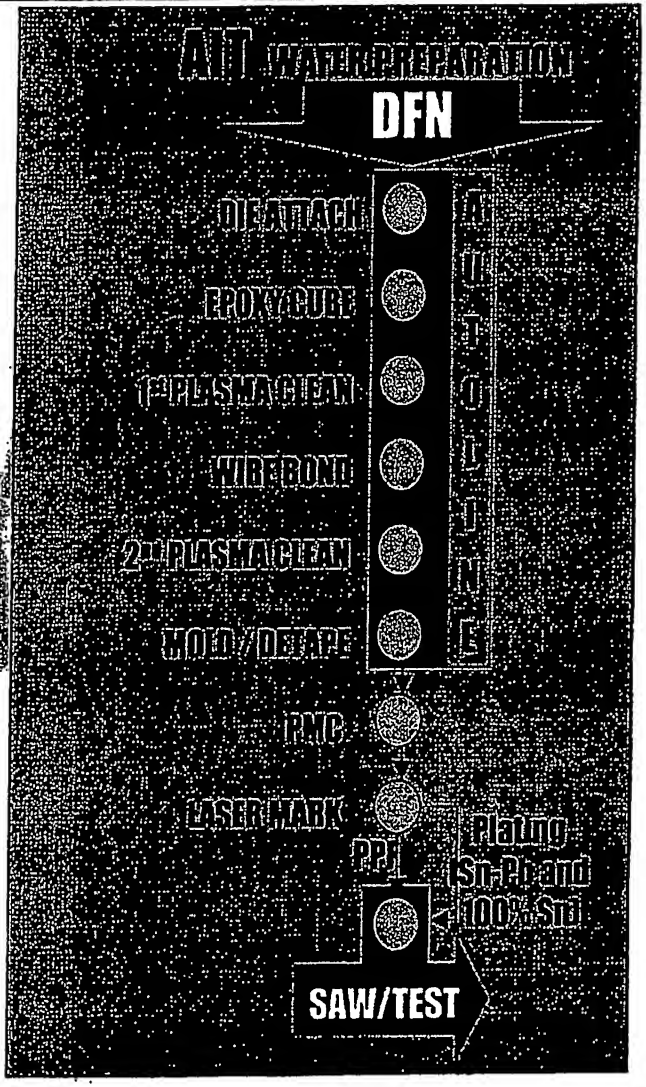
DFN ASSEMBLY LOGISTICS

LEADFRAMES FROM SUPPLIERS

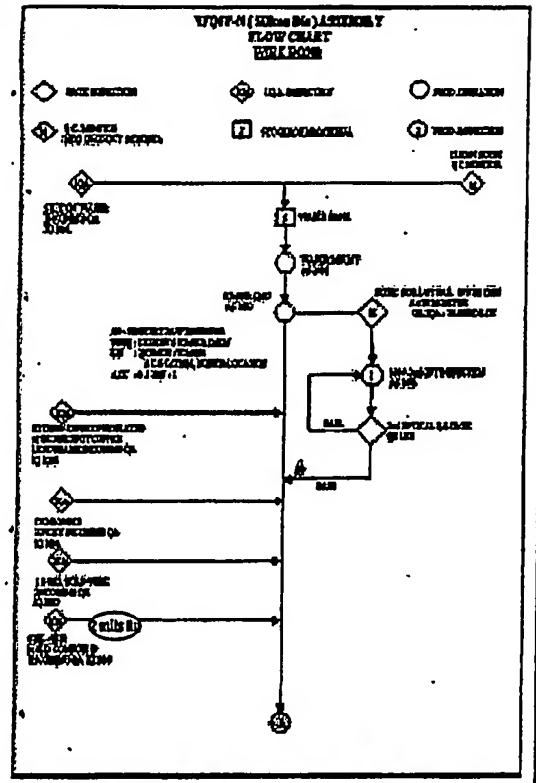


FOLLOW AIT HK PRACTISE

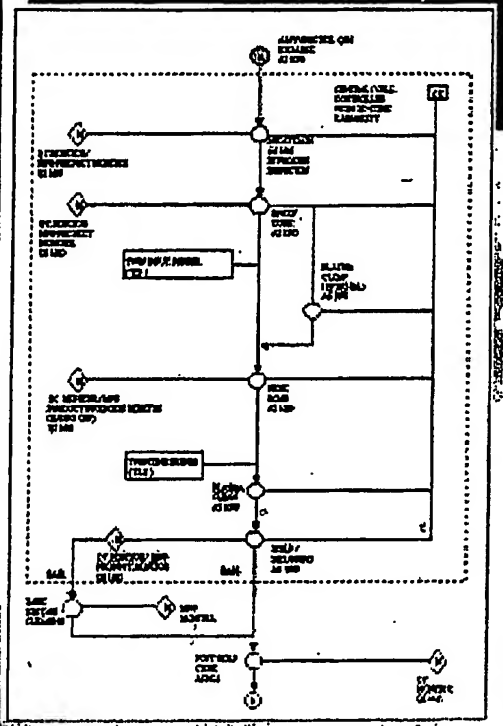
PASSIVES Mounted Lead frames For DFN

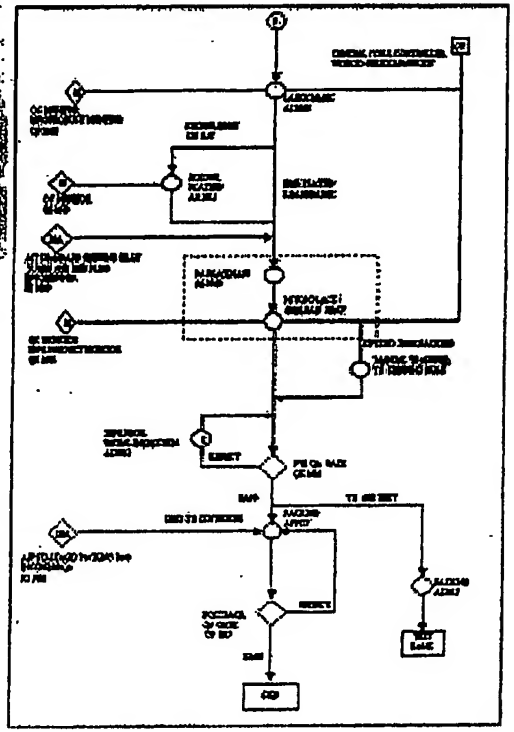


DFN PROCESS FLOW



DFN PROCESS = QFN PROCESS





DFN+ LEAD FRAMES WITH PRE-MOUNTED PASSIVES FOLLOW THE QFN PROCESS AND ASSEMBLY LOGISTICS !!

DFN / DFN+ AUTO-LINES

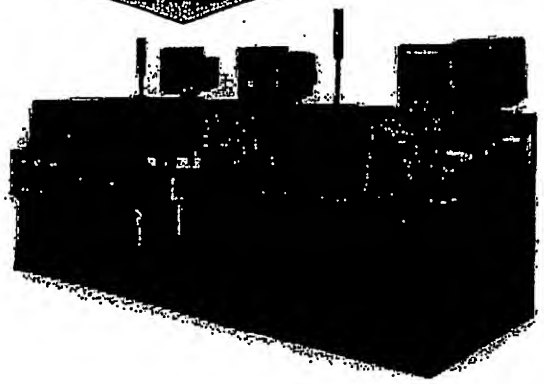
WAFER PREP

DESIGNED AND MADE FOR QFN / DFN ONLY

WIRE BOND

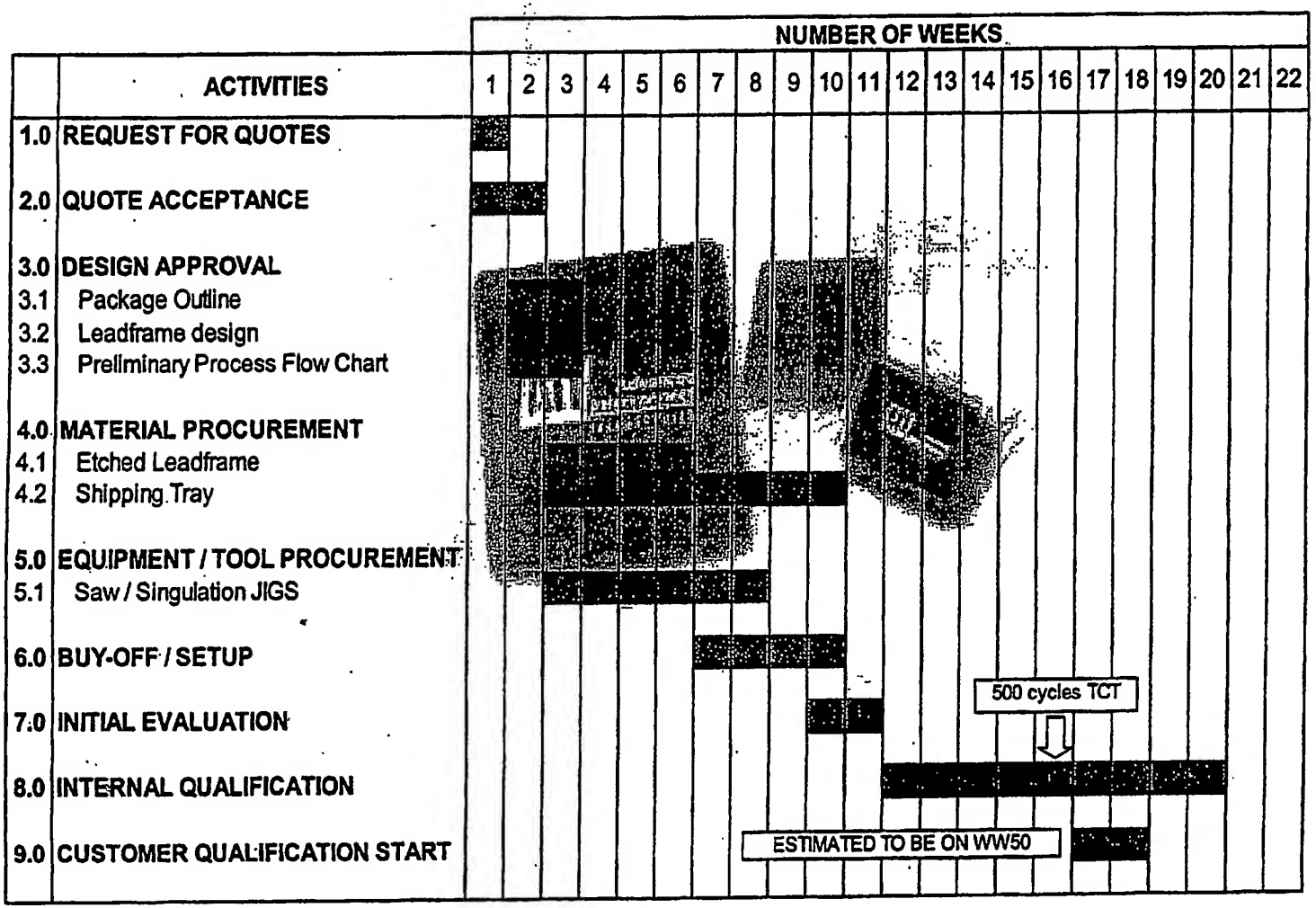
Die-Attach>Snap/Cure> PLASMA>>> WIRE BONDERS >>>> PLASMA> MOLD/De-Tape>>

AFTER MOLD CURE



- ❑ AUTO-LINES FULLY QUALIFIED JULY 2002
- ❑ MULTIPLE BUILDS FOR INTERNAL QUAL
- ❑ CUSTOMER QUALIFICATIONS ON-GOING

DFN / DFN+ TIME-LINE



DFN/ DFN+ SUMMARY

- QFN AUTO-LINES ARE QUALIFIED AND READY FOR DFN / DFN+
- DFN / DFN+ PRODUCTION POSSIBLE IN 16 – 20 WEEKS ARO
- UN-TOOLED FORMAT REQUIRES INITIAL NRE OUTLAY OVER $70K
- PASSIVES TO BE PRE-MOUNTED ON FRAMES BY SUB-CONTRACTOR
- MULTI-DIE DFN+ WITH FEW OR SEVERAL PASSIVES DESIRABLE

While the invention has been described and illustrated in connection with preferred embodiments, many variations and modifications, as will be apparent to those of skill in the art, may be made without departing from the spirit and scope of the invention. By example, it should be appreciated that it is within the scope of the present invention to employ alternate package configurations. For example, the bonding pads 50 may be replaced by leads, similarly bonded to the die 20. In lieu of the encapsulant 70, the package 10 may include an enclosure (e.g., formed by a base and a cap or cover). The plated underside of the die pad may be secured centrally to the upper surface of the base such as via a polymeric adhesive. Various modifications may include plating applied before or after die attachment and/or wire bonding.

Accordingly, the teachings of this invention are not intended to be limited to any specific semiconductor die package arrangement, such as the arrangement described in detail above. As such, the invention as set forth in the appended clams is not limited to the precise details of construction set forth above as such other variations and modifications as would be apparent to one skilled in the art are intended to be included within the spirit and scope of the invention as set forth in the defined claims.

CLAIMS

What is Claimed is:

1. An electronic package, comprising:

a lead frame having a plurality of conductive leads;

a plurality of bond pads;

a semiconductor die mounted to said lead frame and electrically coupled to said bond pads; and

at least one passive component mounted to said lead frame and electrically coupled to said semiconductor die.

2. The package of claim 1 further comprising:

a conductive adhesive, so mounting said semiconductor die to said lead frame; and

a mold compound encapsulating said semiconductor die and said at least one passive component.

3. The package of claim 1 wherein said at least one passive component is selected from the group consisting of capacitors; inductors and resistors.

4. A method for assembling an electronic package, comprising:

providing a lead frame having a plurality of conductive leads;

providing a plurality of bond pads;

electrically and mechanically coupling a semiconductor die to the lead frame and the bond pads;

mounting at least one passive component to the lead frame; and

electrically coupling the at least one passive component to the semiconductor die.

5. The method of claim 4 further comprising encapsulating the bond pads, the semiconductor die, the at least one passive component and inboard portions of the lead frame with an encapsulant.

ABSTRACT

An electronic package is presented including a lead frame having a plurality of conductive leads, a plurality of bond pads, a semiconductor die mounted to the lead frame and electrically coupled to the bond pads and at least one passive component mounted to the lead frame and electrically coupled to the semiconductor die. In one embodiment, the passive component is comprised of one of a capacitor, an inductor and a resistor.

FIG. 1